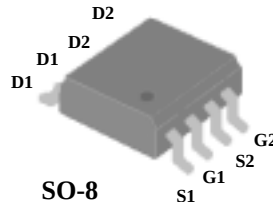




- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Performance

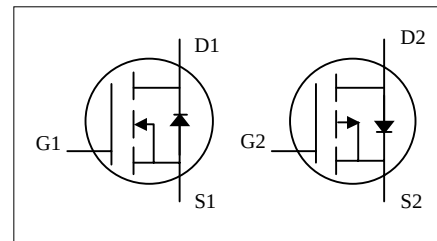


Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

N-CH	BV_{DSS}	35V
	$R_{DS(ON)}$	25m Ω
	I_D	7A
P-CH	BV_{DSS}	-35V
	$R_{DS(ON)}$	40m Ω
	I_D	-6.1A



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	35	-35	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current ³	7	-6.1	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current ³	5.7	-5	A
I_{DM}	Pulsed Drain Current ¹	30	-30	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ\text{C}/\text{W}$



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N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	35	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.02	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =7A	-	18	25	mΩ
		V _{GS} =4.5V, I _D =5A	-	29	37	mΩ
V _{GS(h)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =7A	-	9	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =35V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =28V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =7A	-	11	18	nC
Q _{gs}	Gate-Source Charge	V _{DS} =28V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	6	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =18V	-	12	-	ns
t _r	Rise Time	I _D =1A	-	7	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	22	-	ns
t _f	Fall Time	R _D =18Ω	-	6	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	830	1330	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	150	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	110	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.2	1.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =1.7A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =7A, V _{GS} =0V	-	18	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	12	-	nC

**P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-35	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.02	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-6A	-	32	40	mΩ
		V _{GS} =-4.5V, I _D =-4A	-	50	60	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-6A	-	9	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-35V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-28V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-6A	-	10	16	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-28V	-	2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	6	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-18V	-	10	-	ns
t _r	Rise Time	I _D =-1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =-10V	-	26	-	ns
t _f	Fall Time	R _D =18Ω	-	7	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	690	1100	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	165	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF
R _g	Gate Resistance	f=1.0MHz	-	5.2	7.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-1.7A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =-6A, V _{GS} =0V	-	20	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	12	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 135 °C/W when mounted on Min. copper pad.



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N-Channel

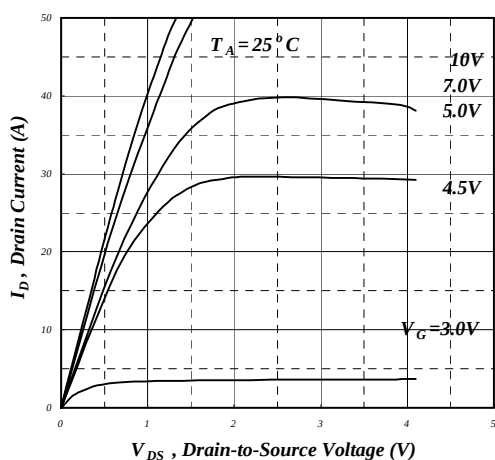


Fig 1. Typical Output Characteristics

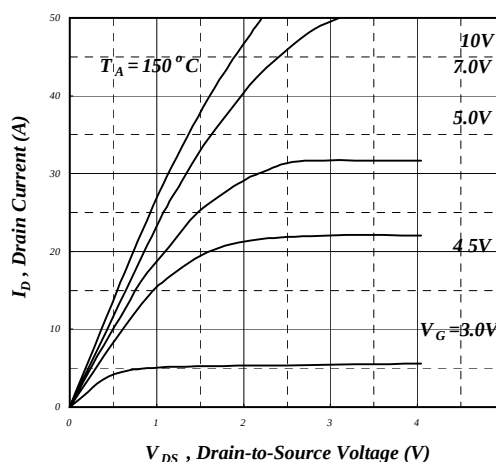


Fig 2. Typical Output Characteristics

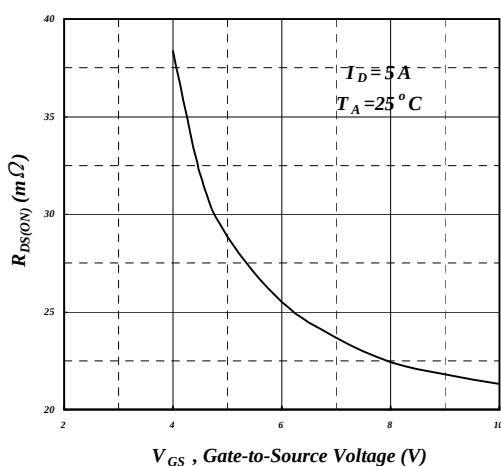


Fig 3. On-Resistance v.s. Gate Voltage

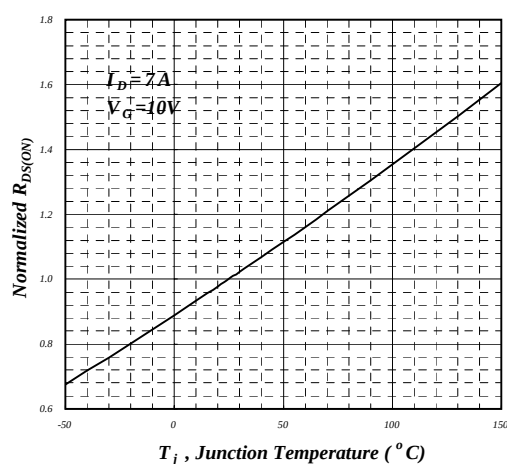


Fig 4. Normalized On-Resistance v.s. Junction Temperature

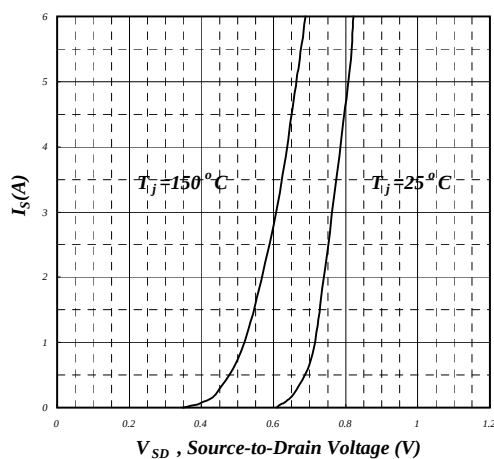


Fig 5. Forward Characteristic of Reverse Diode

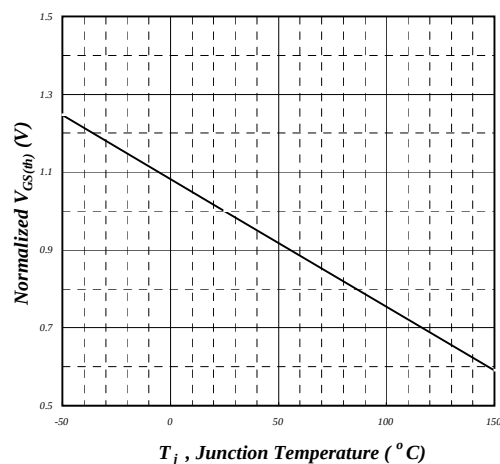


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

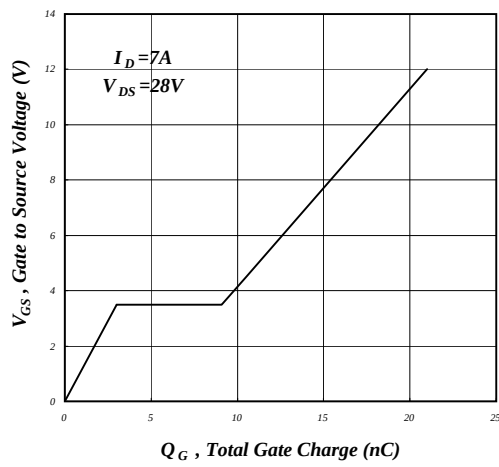


Fig 7. Gate Charge Characteristics

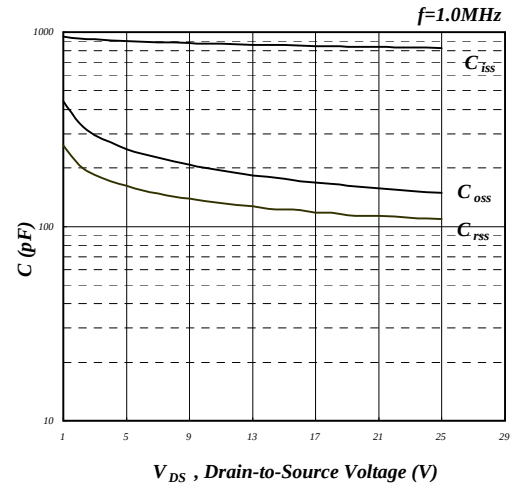


Fig 8. Typical Capacitance Characteristics

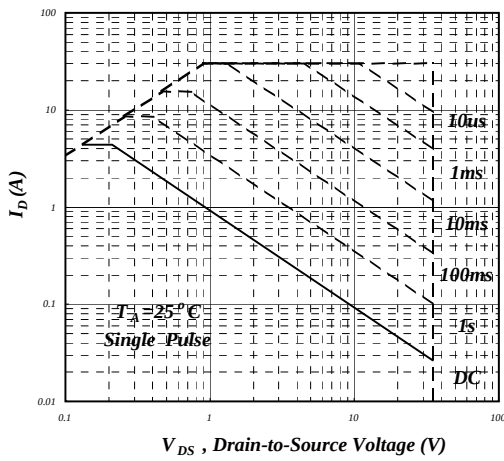


Fig 9. Maximum Safe Operating Area

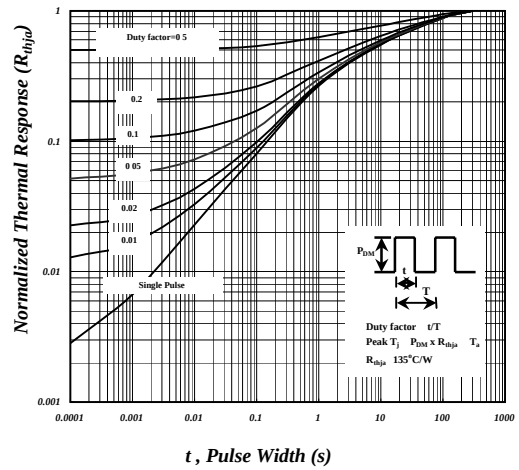


Fig 10. Effective Transient Thermal Impedance

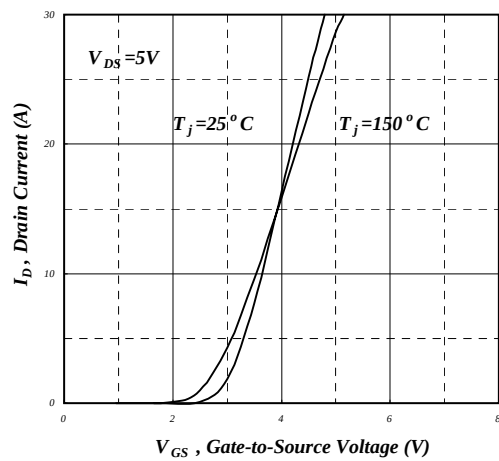


Fig 11. Transfer Characteristics

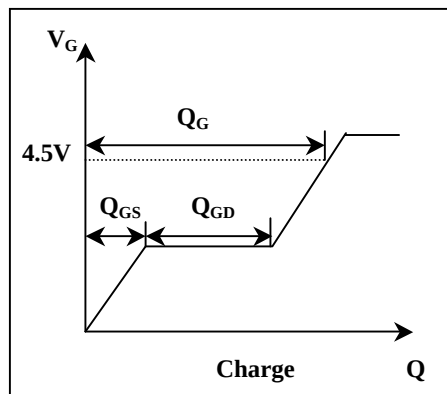


Fig 12. Gate Charge Waveform



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P-Channel

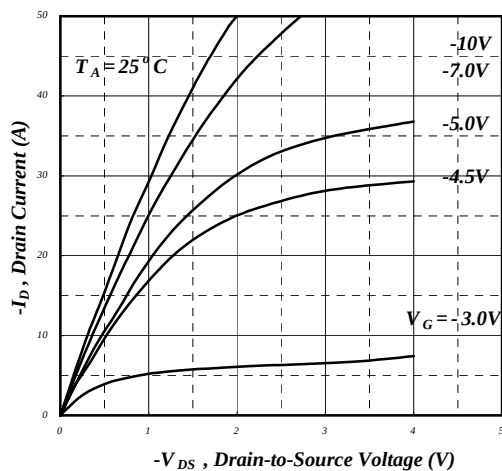


Fig 1. Typical Output Characteristics

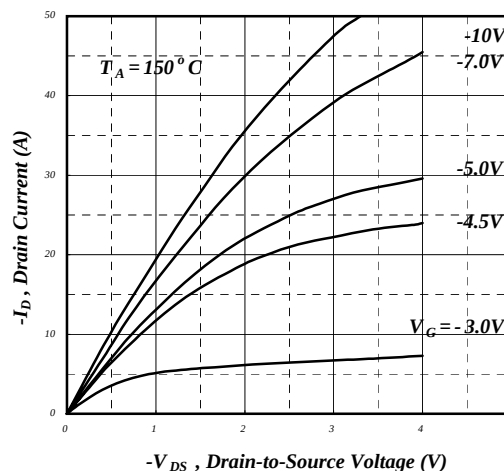


Fig 2. Typical Output Characteristics

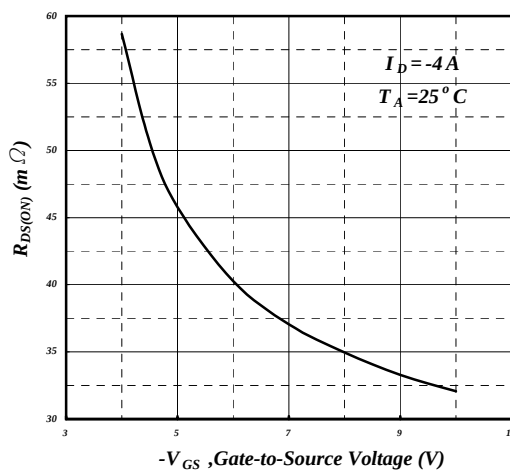


Fig 3. On-Resistance v.s. Gate Voltage

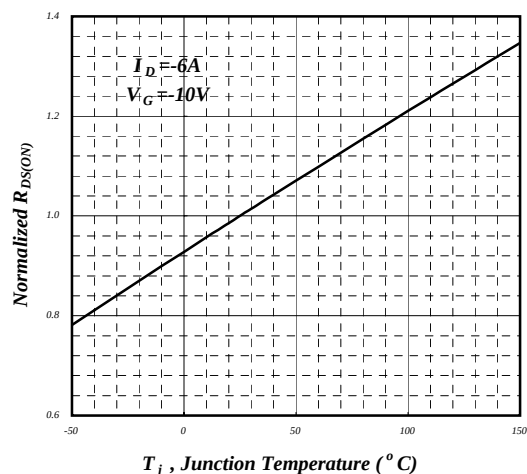


Fig 4. Normalized On-Resistance v.s. Junction Temperature

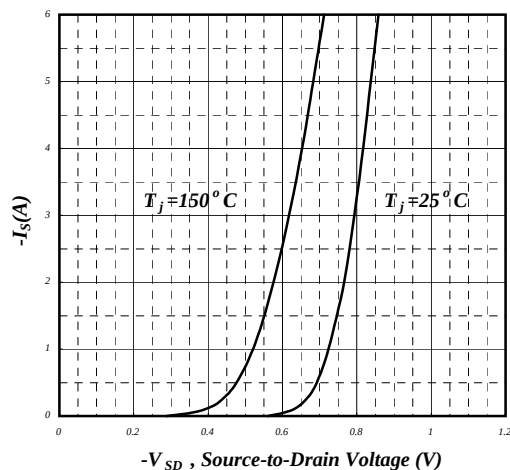


Fig 5. Forward Characteristic of Reverse Diode

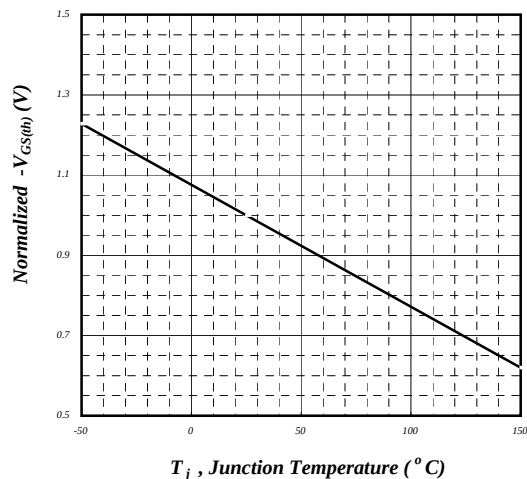


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

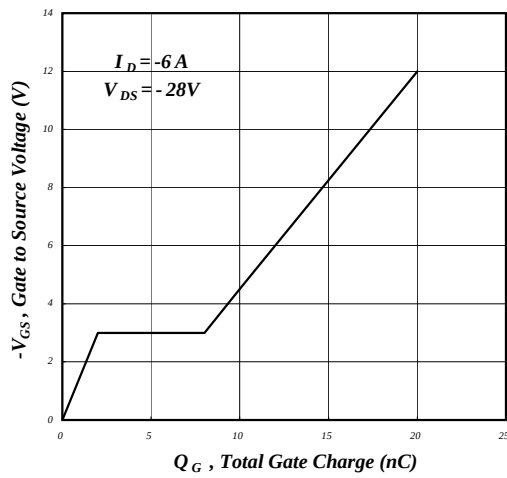


Fig 7. Gate Charge Characteristics

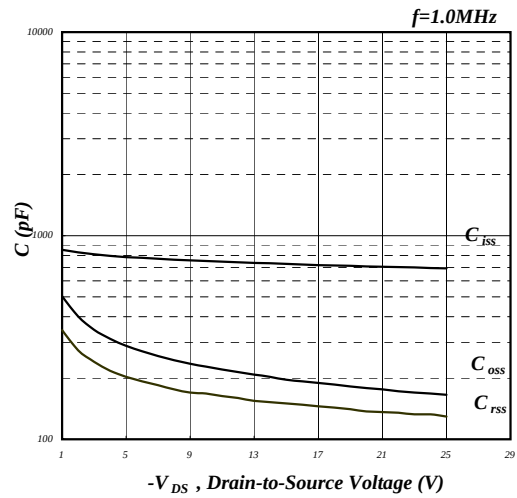


Fig 8. Typical Capacitance Characteristics

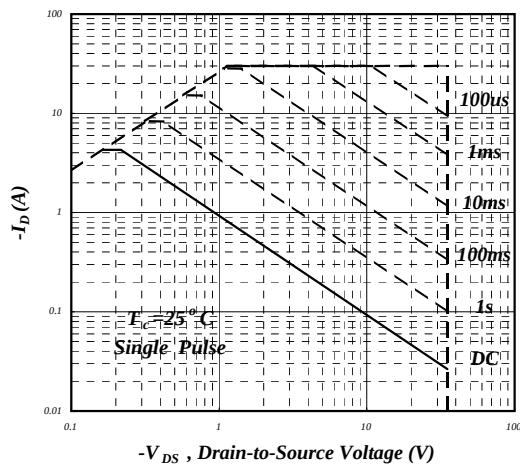


Fig 9. Maximum Safe Operating Area

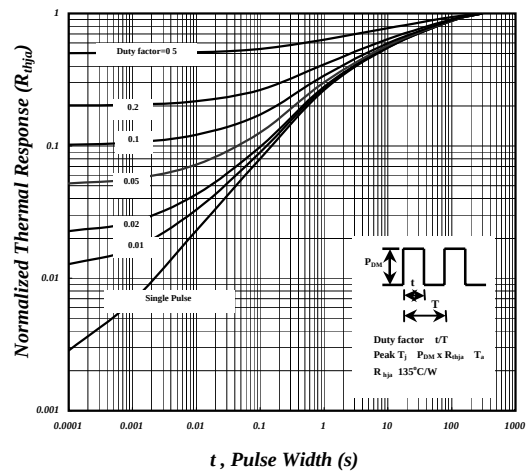


Fig 10. Effective Transient Thermal Impedance

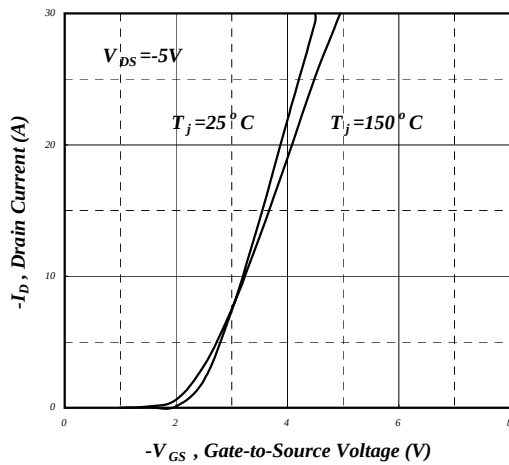


Fig 11. Transfer Characteristics

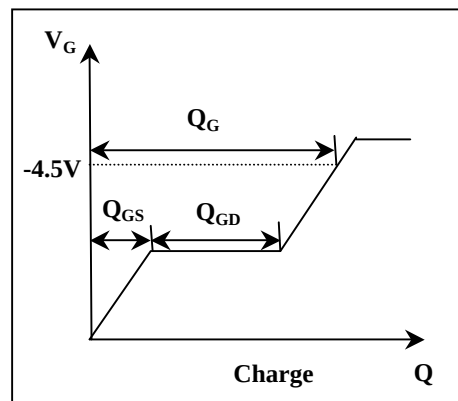


Fig 12. Gate Charge Waveform