Switch-mode Power Rectifier

DPAK Surface Mount Package

MURD320, NRVUD320, **SURD8320**

These state-of-the-art devices are designed for use in switching power supplies, inverters and as free wheeling diodes.

Features

- Ultrafast 35 Nanosecond Recovery Time
- Low Forward Voltage Drop
- Low Leakage
- NRVUD, SURD8 Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant*

Mechanical Characteristics

- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- ESD Ratings:
 - ◆ Machine Model = C (> 400 V)
 - Human Body Model = 3B (> 8 kV)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V _{RRM} V _{RWM} V _R	200	٧
Average Rectified Forward Current (T _C = 158°C)	I _{F(AV)}	3.0	Α
Peak Repetitive Forward Current (Square Wave, Duty = 0.5, T _C = 158°C)	I _{FRM}	6.0	Α
Non-Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, 60 Hz)	I _{FSM}	75	А
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-65 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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ULTRAFAST RECTIFIER 3.0 AMPERES, 200 VOLTS



CASE 369C



MARKING DIAGRAM





MURD320T4G **SURD8320T4G** NRVUD320VT4G

= Assembly Location**

= Year

WW = Work Week

= Pb-Free Package

**The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping [†]
MURD320T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NRVUD320VT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NRVUD320W1T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NRVUD320W1T4G- VF01	DPAK (Pb-Free)	2500 / Tape & Reel
SURD8320T4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MURD320, NRVUD320, SURD8320

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance – Junction-to-Case	$R_{ heta JC}$	6	°C/W
Thermal Resistance – Junction–to–Ambient (Note 1)	$R_{\theta JA}$	80	°C/W

^{1.} Rating applies when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage Drop (Note 2) ($i_F = 3 \text{ Amps}, T_J = 25^{\circ}\text{C}$) ($i_F = 3 \text{ Amps}, T_J = 125^{\circ}\text{C}$)	VF	0.95 0.75	Volts
Maximum Instantaneous Reverse Current (Note 2) (T _J = 25°C, Rated dc Voltage) (T _J = 125°C, Rated dc Voltage)	i _R	5 500	μА
Maximum Reverse Recovery Time $ \begin{aligned} &(I_F=1 \text{ Amp, di/dt}=50 \text{ Amps/μs, $V_R=30$ V, $T_J=25^\circ$C)} \\ &(I_F=0.5 \text{ Amp, } i_R=1 \text{ Amp, } I_{REC}=0.25 \text{ A, $V_R=30$ V, $T_J=25^\circ$C)} \end{aligned} $	t _{rr}	35 25	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width = 300 μ s, Duty Cycle \leq 2.0%.

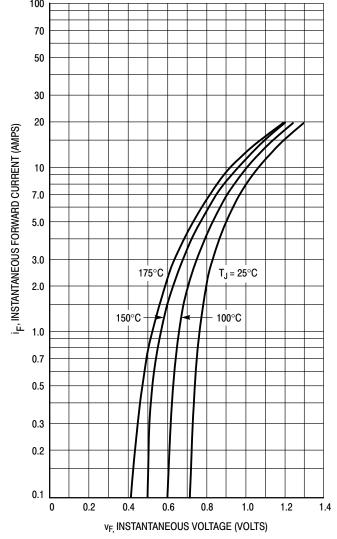


Figure 1. Typical Forward Voltage

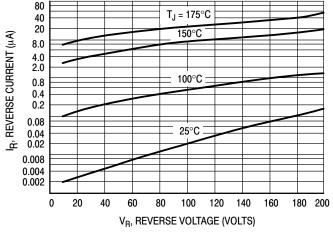


Figure 2. Typical Reverse Current*

* The curves shown are typical for the highest voltage device in the voltage grouping. Typical reverse current for lower voltage selections can be estimated from these curves if V_R is sufficiently below rated V_R .

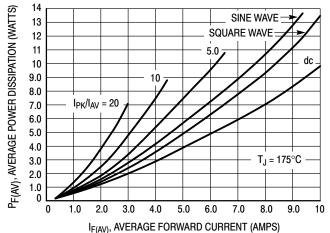


Figure 3. Average Power Dissipation

MURD320, NRVUD320, SURD8320

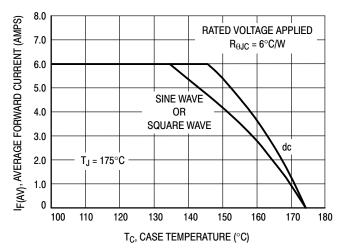


Figure 4. Current Derating, Case

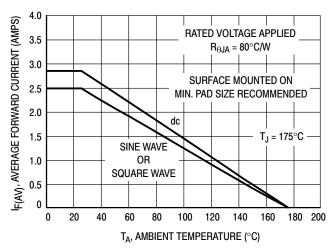


Figure 5. Current Derating, Ambient

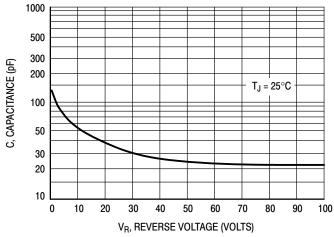
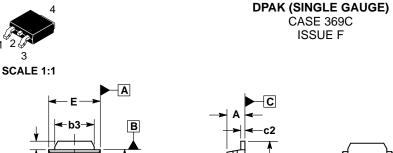
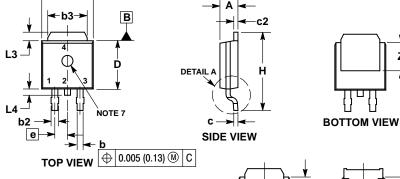
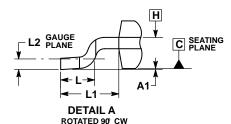


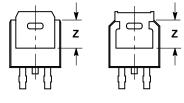
Figure 6. Typical Capacitance

DATE 21 JUL 2015





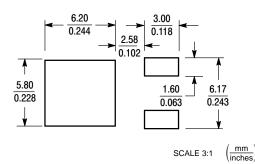




BOTTOM VIEW ALTERNATE CONSTRUCTIONS

STYLE 1: PIN 1. BASE 2. COLLE 3. EMITTI 4. COLLE	ER 3. SOL	AIN 2. CATI JRCE 3. ANO	HODE 2. ANODE DE 3. GATE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6:	STYLE 7:	3. ANODE	STYLE 9:	STYLE 10:
PIN 1. MT1	PIN 1. GATE		PIN 1. ANODE	PIN 1. CATHODE
2. MT2	2. COLLECTOR		2. CATHODE	2. ANODE
3. GATE	3. EMITTER		3. RESISTOR ADJUST	3. CATHODE
4. MT2	4. COLLECTOR		4. CATHODE	4. ANODE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

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- IOTES. 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: INCHES. 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-

- MENSIONS b3, L3 and Z.

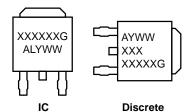
 Jimensions b And E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

 MENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.

 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

		INCHES		MILLIM	IETERS
	DIM	MIN	MAX	MIN	MAX
	Α	0.086	0.094	2.18	2.38
	A1	0.000	0.005	0.00	0.13
	b	0.025	0.035	0.63	0.89
ĺ	b2	0.028	0.045	0.72	1.14
	b3	0.180	0.215	4.57	5.46
	С	0.018	0.024	0.46	0.61
	c2	0.018	0.024	0.46	0.61
	D	0.235	0.245	5.97	6.22
	Е	0.250	0.265	6.35	6.73
	е	0.090	BSC	2.29	BSC
	Н	0.370	0.410	9.40	10.41
	L	0.055	0.070	1.40	1.78
	L1	0.114	REF	2.90	REF
ĺ	L2	0.020	BSC	0.51	BSC
	L3	0.035	0.050	0.89	1.27
	L4		0.040		1.01
	Z	0.155		3.93	

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code = Assembly Location Α L = Wafer Lot Υ = Year

WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

DOCUMENT NUMBER:	98AON10527D	E
STATUS:	ON SEMICONDUCTOR STANDARD	a ve
NEW STANDARD:	REF TO JEDEC TO-252	"(
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOU	NT

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PAGE 1 OF 2



DOCUMENT	NUMBER:
98AON10527	7D

PAGE 2 OF 2

ISSUE	REVISION	DATE
0	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
Α	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
В	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
С	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

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